



EISCAT

THE RACELAN LANGUAGE

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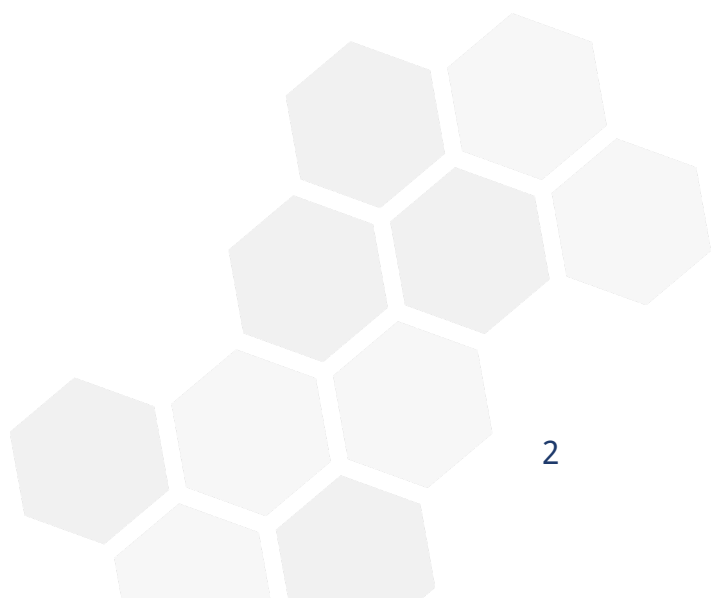
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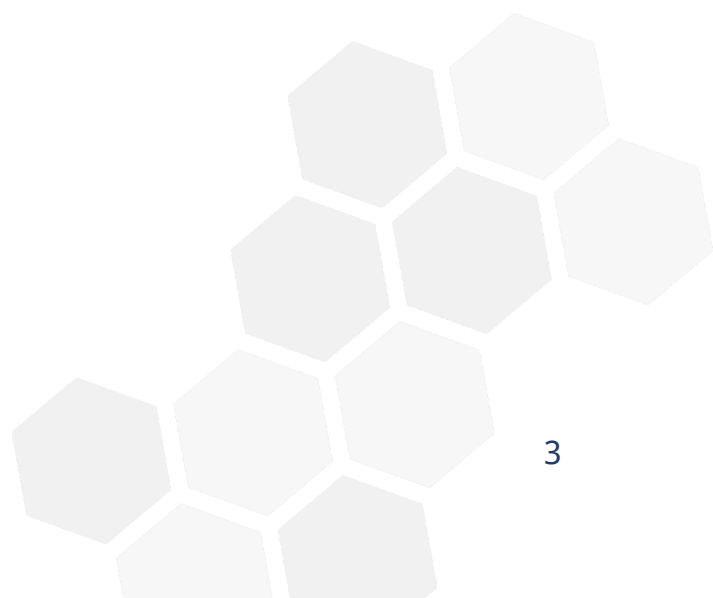
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The Racelan Language

The manual for the original radar controller compiler for ESR, racelan can be found [here](#). A new radar controller compiler is now available which is called tarlan_esr. This version is especially made for the new DSP system installed in the summer of 2002. The manual for the racelan compiler will also cover the tarlan_esr compiler except some small differences shown below.

1. Racelan commands not implemented

tarlan_esr

INCTCR

DO n/ ENDDO

ADCTRIGON

ADCTRIGOFF

DEF

SYMB_NAME

SETCOUNT

New or duplicated command

racelan <-> tarlan_esr

BUFLIP1 <-> BUFLIPI Note: For the ION line DSP box only BUFLIP is implemented. Please look at the ESR receiver block diagram.

BUFLIP2 <-> BUFLIPII Note: BUFLIPII and BUFLIP2 is only implemented in plasma line DSP

ENABM[1-6] <-> CH[1-8]

DISBM[1-6] <-> CH[1-8]OFF

RXBITON[0-31] <-> BRX[0-31]

RXBITOFF[0-31] <-> BRX[0-31]OFF

TXBITON[0-31] <-> BTX[0-31]

TXBITOFF[0-31] <-> BTX[0-31]OFF

AD[1,2][L,R] Set proper AD selection for the channel boards. For example AD1L, route input for AD 1 to channel board 1, 2, 3. AD2R, route AD 2 to channel 4, 5, 6. This is for the ION line box. For the plasma line box we have the split channels as 1-4 and 5-8.

NCOSSEL[0-1023] Load the frequency defined in the requested memory into the NCO on the channel board.

IF2[AB] Is gone, as the switch for selecting plasma line channel is removed.

HBRX[0-5] Set a bit in the high bit field in the receiver radar controller

HBRX[0-5]OFF Unset a bit in the high bit field in the receiver radar controller

HBTX[0-5] Set a bit in the high bit field in the transmitter radar controller

HBTX[0-5]OFF Unset a bit in the high bit field in the transmitter radar controller

CAUTION! No sanity checks are done on direct bit manipulations done with BRX[0-31], BRX[0-31]OFF, BTX[0-31], BTX[0-31]OFF, HBRX[0-5], HBRX[0-5]OFF, HBTX[0-5], and HBTX[0-5]OFF. These commands should be used with great care.

New commands for the plasma line receiver chain

STFIRP	Start fir filter. Ion line command STFIR
RXSYNCPON	Rx sync on. Ion line command RXSYNCON
RXSYNCPOFF	RX sync off. Ion line command RXSYNCPON
NCOPRSP	Reset phase registers on NCO's. Ion line command NCOPRS
STCP	Send start compute interrupt. Ion line command STC
AD[1-2]LP	Route proper AD to channel boards. Ion line command AD[1-2]L
AD[1-2]RP	Route proper AD to channel boards. Ion line command AD[1-2]R
CH[1-8]P	Start channel board memory writing. Ion line command Ch[1-8]
CH[1-8]POFF	Stop channel board memory writing. Ion line command CH1[1-8]OFF
ALLPOFF ALLOFF	Stop channel board memory writing on all channels. Ion line command
NCOSSEL[0-1023]P	Use a NCO memory location. Ion line command NCOSSEL[0-1023]

BRX[0-31]P	Set a specific bit in the plasma radar controller. Ion line command BRX[0-31]
BRX[0-31]POFF	Unset a specific bit in the plasma radar controller. Ion line command BRX[0-31]OFF
HBRX[0-5]P	Set a specific high bit in the plasma radar controller. Ion line command HBRX[0-5]
HBRX[0-5]POFF	Unset a specific high bit in the plasma radar controller. Ion line command HBRX[0-5]OFF

AD[1-2]PLA[3-4]2M[U,D] Route plasma IF channels to proper AD converter, for example AD1PLA32MU will route 32m upshifted IF channel to AD1

These new commands can be used directly inside the tlan code for the 32m antenna, the compiler will give three binaries out. These will be called, for the transmitter xxx_esr.tbin, for the ion line xxx_ionesr.rbin and for the plasma line xxx_plasmaesr.rbin. These binaries can now be loaded in the proper radar controller from the ELAN file. As an example [steffe@32m.tlan](#) is shown.

2. The tarlan_esr Compiler

tarlan_esr [SWITCHES] [OPTIONS] file_name

2.1. Options

-f <file name>

2.2. Switches

-p Switch, to compile for the old DSP crate which is used for the plasma lines. This box have an 10 MHz AD.

The default is to compile for the ion line DSP crate. In this box the AD operate at 15 MHz.

-c Switch, to enable Chx sample window timing output. Example:

<>tarlan_esr -c -f /kst/eros4/exp/arc_slice/

2.3. Compiling for ESR

Will write to rx file arc_slice_esr.rbin

Will write to tx file arc_slice_esr.tbin

CH1=3030 us

CH2=120 us

CH1=3030 us

CH2=120 us

CH1=3030 us

..... Output cutted here

Total channel on time at BUFLIP

CH1 387840.0 us on CH2 15360.0 us on CH3 0.0 us on CH4 0.0 us on CH5 0.0 us on CH6 0.0 us on
BUFLIPCH1=3030 us

CH2=120 us

..... Output cutted here

RFON=98304 us IPP=1009920 us rf duty=9.73% beam duty=11.28% rxprot duty=13.03%

Longest pulse 384 us

Shortest pulse 384 us

Nr of instr TX=10896 RX=1038

Bytes in controller prog. 0 RX=8320 and TX=87152

Bytes in tx file 87152

Bytes in rx file 8320

3. Imposed hardware timing limits and default bit patterns

```
% These are the hardware delay times for the ESR radar.
% The delay times are given in usecs.
% This file is used by the tarlan_esr compiler.
%
% 10-May-2002: Default RXBITPATTERN 0x4007FE80 --> 0x4007FEC0
%
% Minimum, maximum rf duty cycle
%
RFDUTYCYCMIN 0.1 % (%)
RFDUTYCYCMAX 25.0 % (%)
%
% Minimum, maximum RF pulse lengths
%
RFPULSEMIN 0.5 % (us)
RFPULSEMAX 2000 % (us)
%
% Maximum BEAMON time
%
BEAMONMAX 2000 % (us)
%
% Minimum, maximum beam duty cycle
%
BEAMDUTYCYCMIN 0.1 % (%)
BEAMDUTYCYCMAX 25.0 % (%)
%
% Minimum, maximum beam ipp
```

```

%
BEAMIPPMIN 500 % (us)
BEAMIPPMAX 50000 % (us)
%
% Maximum RXPROT duty cycle
%
RXPROTDUTYCYCMAX 40.0 % (%)
% HARDWARE TIMINGS FOR TRANSMITTER
RXPROT->BEAMON 10 % RXPROT until BEAMON can be given (us)
BEAMON->RFON 10 % BEAMON until RFON can be given (us)
PREAMPOFF->BEAMON 10 % Shortest time between PREAMPOFF and BEAMON (us)
RFOFF->BEAMOFF 5 % RFOFF until BEAMOFF can be given (us)
BEAMOFF->RXPOFF 20 % BEAMOFF until RXPOFF can be given (us)
RXPOFF->PREAMPON 5 % Shortest time between RXPOFF and PREAMPON (us)
% HARDWARE TIMINGS FOR DSP
% STC until END can be given
STC->END 15 % Ion DSP (us)
STCP->END 15 % Plasma DSP (us)
% longest time between STC and BUFLIP
STC->BUFLIP 5 % Ion DSP (us)
STCP->BUFLIP 5 % Plasma DSP (us)
%Default bit pattern for the radar controllers
% The TXBITPATTERN and RXBITPATTERN are in hex
RXBITPATTERNPLASMA 0x4007FCD0 % Default bit setting for the plasma side
RXBITHPATTERNPLASMA 0x3F % High default bit setting for the plasma side
RXBITPATTERNION 0x4007FE80 % Default bit setting for ion side
RXBITHPATTERNION 0x3F % High default bit setting for the ion side
TXBITPATTERN 0x07FBFFF8 % Default bit setting for the transmitter
TXBITHPATTERN 0x0 % Default high bit setting for the transmitter
%
```

END

